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Proton Irradiation Effects on 2Gb Flash Memory

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Abstract—**We report total ionizing dose and single event effects on 2Gb Samsung flash memory devices after exposure to 200 MeV protons to various doses up to 83 krad(Si). We characterize observed failures and single event upsets on 22 devices from two different lots. Devices from both lots are robust to greater than 20 krad(Si) although we see evidence for lot-to-lot variation where only one lot appears robust up to about 50 krad(Si). Single event upsets are observed at a relatively low rate and are consistent with single isolated bit flips within registers that transfer bits to and from the flash memory cells.**

I. Introduction

We describe a study of proton radiation effects on dense flash memories in order to determine whether these devices could be considered for use in a mass memory system for a space-based telescope observatory. Our results are affirmative in that all the tested devices suffered no catastrophic effects to a dose of 20 krad(Si). Others seeking to find high capacity, low power, nonvolatile memory for space or other radiation applications, where the total dose requirement is relatively low, may wish to consider the device under test or similar devices.

The SuperNova/Acceleration Probe (SNAP) [1] is a proposed space observatory to study dark energy as part of a DOE-NASA Joint Dark Energy Mission. SNAP seeks to collect and measure 2000 Type Ia supernovae in order to study the acceleration of the universe. The current design of the SNAP focal plane [2] has 36 optical CCDs and 36 infrared detectors that contribute to a total channel count of approximately 600 million pixels. Initial designs call for a mass memory system on board that stores image data prior to transmittal to a ground station. A solid-state memory system has advantages of no moving parts that might otherwise be points of failure or make attitude control systems more complex. The large number of pixels and the number of planned images recorded before telemetry drives the requirement for the size of the mass memory to the few Tbit range. Thus, only commercial memory technologies that are dense such as flash or DRAMs are currently viable. Constraints on the overall power budget for the observatory become less severe if the mass memory requires as little power as necessary. Flash memory is a nonvolatile memory that requires relatively little power when compared to other technologies. Thus, we are exploring whether flash might be an appropriate technology for SNAP and other similar space flight applications.

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Flash memory has been used on spacecraft missions in the past, but not at the size and scale required by SNAP. The suitability of flash for space flight has also been called into question based upon previous measurements that have shown catastrophic failures to radiation at total ionizing dose levels of less than 20 krad(Si) [3] where the likely point of failure was the internal charge pump that provides an internal high voltage for write and erase operations. The SNAP satellite is planned to be located in an orbit near the L2 Lagrange point where the radiation requirements for electronics behind shielding will most likely require tolerance at least to 20 krad(Si). We recognize that effects due to radiation damage may depend on scaling with feature size and device architecture and that modern dense flash devices may have different susceptibilities to various radiation damage mechanisms compared with previous generations of such devices.

II. Experimental Details

A. Description of the device under test

The Samsung 2Gb flash device, part no. K9K2G08U0M, was chosen for this study since it had the largest capacity of readily available devices at the time we started procurement for this investigation. The device consists of two die within a single package and consists of NAND flash memory cells arranged in a 256M x 8-bit configuration. The memory is segmented into 2048 blocks that contain 64 pages of 2048 (plus 64) bytes. We tested devices originating from two different lots with date codes 328 (Lot 1) and 410 (Lot 2).

B. Measurement Apparatus

We have produced printed circuit boards to which the memory devices may be mounted. The printed circuit board locates the device to be tested in the center of a 5 in. x 5 in. area that is to be exposed to radiation where the beam spot size is concentrated on an area of radius approximately 2 in and falls to a few percent of the peak intensity by 4 in. Traces from the flash memory connect with other components outside of this 5 in. x 5 in. area. These other components include LVDS transceivers, some logic to prevent conflicts on the bi-directional 8-bit bus, termination resistors, and cable connectors. The printed circuit board with the components allow for control and communication to the flash device over a 15 ft. long twist and flat cable to a computer data acquisition system (DAQ). The DAQ consists of a Pentium based computer running Linux with a PCI Test Adapter (PTA) card and with four Programmable Mezzanine Cards (PMCs)

developed at Fermilab. It is the PMC that receives the data cable going to the flash printed circuit board and so up to four flash devices may be controlled simultaneously. The PTA and PMC cards have programmable FPGA chips that have been configured to pass through control and other communication to the flash device using programmed registers. Software has been written in C to control these registers and thus to control the flash device under test. A graphical user interface written in JAVA provides access to the flash memory chip control software through convenient buttons and display windows. The DAQ system was located behind shielding and was connected via a 15 ft. long cable to the device under test.

The printed circuit board also contains a connector that carries separate power to the external components and the flash device under test. A low voltage power supply provides the basic power that is distributed through custom cards that provide power regulation, over-current shut-off, and a monitoring output that was connected to a programmable interface card (PIC) for digitization of the current drawn by the flash device. In the radiation study, the power supply and power distribution system was located in a control room through 50 feet of cable to the flash printed circuit board. Also in the control room, a computer remotely controlled the DAQ computer over an Ethernet connection.

C. *Radiation Facility*

The Indiana University Cyclotron Facility (IUCF) provides proton irradiation as part of a Radiation Effects Research Program (RERP) [4]. Proton beams to 200 MeV in energy are available. The fluence for each running period could be specified and dose rates from approximately 1 to 100 krad(Si)/hr. were used in this study. Dosimetry was provided by the facility using a calibrated Faraday cup and secondary electron monitor. The beam profile at the target was measured using an exposed film, which showed the entire area of the packaged device received uniform radiation exposure to within 5%. Our estimate is that the absolute value of the quoted radiation dose in this study is accurate to within 10%. We performed our measurements at IUCF on two dates – in November 2003, where we tested six devices from the first lot, and in May 2004, where we tested four devices from the first lot and twelve devices from the second lot.

III. FIRST RADIATION TESTING AND RESULTS

A. *Test Procedure*

The first radiation testing consisted of two running periods. In the first running period, a single flash device was exposed to 83Krad(Si) of 200 MeV proton irradiation over the course of approximately six hours. The device was powered and exercised by looping over each of the 2048 blocks multiple times in an erase-write-read (EWR) cycle. The cycle began with a block erase command after which a read and compare of 'FF' data (expected content after an erase) was performed for 64 pages times 2048 bytes. If the comparison failed, an "erase error" was noted. The cycle continued with a write of 'F0' into each of the 64 pages times 2048 bytes of the block. A read and compare was then made to complete the cycle. If this comparison failed, a "read error" was noted and the content of the byte and address location of the failed byte was noted. During the EWR cycle, asynchronous measurements were made of the current drawn by the flash device. The current measurements were recorded once per EWR cycle and written into an online data stream that also recorded erase and read errors.

In the second running period, five boards were simultaneously exposed to the proton beam with the boards stacked close to one another to a total dose of 36 krad(Si) over the course of approximately 3 ½ hours. Each of the five boards was operated in a different mode. Boards 1 through 4 were connected to PMC cards and were exercised during the radiation exposure again by looping over the 2048 blocks of the device. Board 1 was initialized with a checkerboard 'F0' pattern written into every byte. A read operation and comparison was made for all the bytes in the block. Read errors were recorded. Board 2 was initially erased so that every memory cell contained 'FF'. Four writes were performed so that each cell subsequently contained 'F7', 'F3', 'F1', and then 'F0'. The error status of the write command was monitored although we never observed an error being flagged through this status line. Board 3 was exercised after being initialized with 'F0' everywhere with a block erase operation followed by a read and compare for 'FF'. Erase errors were recorded. In addition, the erase error status line was monitored although no errors on this status line were observed during our testing. Board 4 was exercised in the same manner as the board from the first running period. This board was in a cycle of EWR with errors being flagged as discussed above. The final board was preloaded with 'F0' and was exposed to 12 krad(Si) with no power being supplied to the board and then it was exposed to 24 krad(Si) with power but no other operations. In this sense, it was in a static mode. The contents of its memory cells were examined at a later time.

B. *Results from the first radiation testing*

For the first radiation testing, no device suffered a catastrophic failure. The device exposed to 83 krad(Si) did incur a 30% increase in current after 44 krad(Si) but continued to operate normally. At 59 krad(Si), the device stopped working. After a power cycle to the device, it began to operate normally and draw the original typical current. This incident is consistent with a single event functional interrupt (SEFI). The four boards that were exercised to 36 krad(Si) did so normally with no noticeable change in current draw. The fifth board that was preloaded and not exercised during exposure operated normally when it was examined and tested after the radiation exposure.

Single event upsets were studied by examining bits that were read back from the device under test and comparing with expectation. A total of three hundred thirty-nine errors were recorded during the irradiation for all the tested boards, which extrapolates to a low rate given the relatively high dose rates. Each error appeared to be a single occurrence of a random upset of a single bit. All of these errors are consistent with being single event upsets (SEUs) in either the flash memory registers used to buffer data before writing into the memory

cells or in registers used to buffer data after extracting it from the memory cells. When memories were examined during beam-off conditions after irradiation, no errors were ever found as would be expected if upsets had occurred within the core of the flash memory. Read errors were recorded that were not found when the same memory location was examined in beam-off conditions, which also indicates the upset occurring in the registers as opposed to occurring in the core of the memory. Single event upsets were characterized as either 0->1 or 1->0 upsets, which were found to occur with nearly equal probability. Similarly, each possible location of a bit in the 8-bit data word was also found to be nearly probable to being upset. The rate of upsets was proportional to the flux; however, a cross section for upsets has not been computed and would be ill defined since the rate would also depend upon the speed at which the device was operated.

Figure (1) shows the number of errors observed as a function of the number of EWR cycles for the board irradiated to 83 krad(Si). During the irradiation, the flux was increased from 7×10^6 to 8×10^8 cm^2/s. The total number of cycles over all the blocks corresponds to roughly 5×10^9 chip operations. The total number of errors observed was 271 and were distributed over many individual periods where the beam flux was increased. The observation that the upsets appeared as single bit upsets and were isolated indicates that error detection and correction algorithms should be able to correct for these rare bit flips for use by SNAP.

A long duration test of a device was performed with no beam for 193 hours (~8 days) in an EWR cycle. No errors were recorded for the 8×10^{11} bits that were examined.

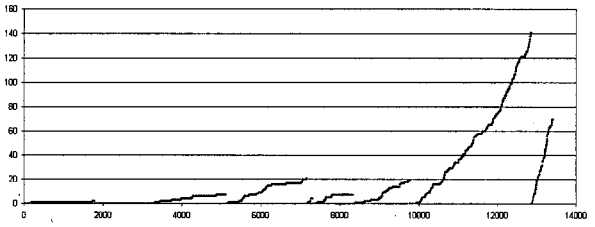

Figure 1. Number of SEUs observed as a function of EWR cycle (1 per block) during the course of an 83 krad(Si) exposure. The error counter was reset to zero when beam parameters, such as the flux, was varied from 7×10^6 to 7×10^8 cm^2/s over the course of the running period.

IV. SECOND RADIATION TESTING AND RESULTS

A. *Test Procedure*

A second round of radiation testing was performed after the results from the first testing were analyzed. The primary goals of the second radiation testing were to increase the statistics in terms of the number of devices tested, look for lot-to-lot variations, and to operate these devices mostly in a static mode since in normal operation on the satellite, each memory cell would typically be erased and written to once per day. The data would be held until the memory would be read out for transmittal to earth. For the second radiation testing, a total of sixteen boards were irradiated. Groups of four boards were irradiated to doses of 75 krad(Si), 50 krad(Si), 20 krad(Si), and 50 krad(Si). Except for four Lot 1 boards used during the last 50 krad(Si) irradiation, all the devices came from the second lot. All of the boards were configured with an initial checkerboard 'F0' pattern before irradiation. During the radiation exposure, one board out of four was actively exercised at a time while the others were in a static configuration just holding their memory contents. When failures were observed, boards were checked and exercised to acquire data.

B. *Results from the second radiation testing*

The full analysis of the data taken during the second radiation testing period is in progress at the time of this writing. However, all the devices have been examined for functionality and some additional measurements have been made that will be described. Boards which had failures had most, if not all (depending on the board), memory locations unable to properly be erased and then written.

To examine functionality, the boards were exercised after irradiation by (1) examining the current contents of the memory, (2) erase the memory and verifying successful erasure, (3) write to the memory a 'F0' pattern and verify. Boards were also cycled in an EWR sequence. We find lot-to-lot differences in terms of functionality. For Lot 1, two out of the four boards irradiated to 50 krad(Si) appear to be fully functional and two had failures. For Lot 2, all four boards irradiated to 20 krad(Si) appear to be fully functional. The four boards to 50 krad(Si) and the four boards to 75 krad(Si) have failures. All the boards continue to power, return a device code when queried, and have memory contents that can be read. The failures occur during erase and write operations consistent with problems in the charge pump.

The examination of the boards occurred approximately one month after the radiation exposure where room temperature annealing may have occurred. We looked at the effects of high temperature (100 C) for 2-6 hr after the initial examination for functionality was made. The chip was biased during the exposure to the high temperature. For the two boards from Lot 1 that had failures after 50 krad(Si), one board recovered full functionality after high temperature annealing. The other Lot 1 board recovered full functionality in all but four of the 2048 blocks after high temperature annealing. Two boards from Lot 2 that had failures after 50 krad(Si) showed no noticeable recovery after annealing at high temperature.

The static (stand-by current I_{SB2}) current draw of each device has been measured before irradiation, immediately after irradiation, and after annealing for approximately 1 month at room temperature. All devices showed a standby current of approximately 15 μA prior to irradiation compared with a value of 20 μA in the datasheet. Immediately after irradiation, devices showed an increase in the current drawn although always less than the maximum value of 100 μA in the datasheet for the device. Boards to 20 krad(Si), 50 krad(Si), and 75 krad(Si) had static currents measurements of 16, 19, and 36 μA respectively. After 1 month of annealing, typical currents reduced to 15, 18, and 25 μA respectively.

The full analysis of single event upsets for the second radiation testing has not yet been performed. However, the error rates and the evidence that such upsets were occurring in the registers and not within the core memory appears to also hold for the Lot 2 devices and appears consistent with the observations from the first radiation testing.

V. CONCLUSIONS

We have described our initial study of 2Gb Samsung flash memory devices when exposed to 200 MeV protons. Total ionizing dose effects from 20 to 83 krad(Si) have been tabulated. All devices tested remain functional to 20 krad(Si). Devices from a Lot 1 remain functional to a dose as high as 83 krad(Si). Two out four devices taken to 50 krad(Si) were functional after irradiation. The other two devices recovered most of the functionality after a brief high temperature annealing period. Devices from Lot 2 appear to be less robust and seem to fail functionality between 20 and 50 krad(Si). In cases of functional failure, the failure occurred in areas of the chip responsible for erase and write operations. Devices that had failures were still able to return their device code and were able to have their memory cells examined. Two of the devices from Lot 2 were also exposed to high temperature but showed no noticeable improvements.

Several hundred SEUs were observed and are consistent with upsets occurring in the write and read registers as opposed to occurring in the core flash memory. Based upon earlier studies of flash devices, we were surprised at the relative robustness of these parts. We plan to continue the analysis of the data which we collected and perform follow-up studies to further characterize the radiation tolerance of these devices and their suitability for space missions. However, based upon the fact that no catastrophic failures occurred at a dose of 20 krad(Si), we find these flash memory devices worthy of further consideration for use in space missions.

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